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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/524,778	02/16/2005	Shigeru Umeno	ABE-026	8727

7590 07/26/2007

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EXAMINER	
MALEKZADEH, SEYED MASOUD	
ART UNIT	**PAPER NUMBER**
1722	

MAIL DATE	DELIVERY MODE
07/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/524,778	UMENO ET AL.	
	Examiner	Art Unit	
	SEYED MASOUD MALEKZADEH	1722	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20-22,24-26,28-30,32-34,36-38 and 40-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20-22,24-26,28-30,32-34,36-38 and 40-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :02/16/2005, ~~11/20/2006~~, 03/16/2007, 04/12/2007..
2-16-05

DETAILED ACTION

New Grounds of Rejection

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 20 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fusegawa et al. (US 2003/0106484) in view of prior art submitted by the applicants JP (2003-297840).

Fusegawa et al. (US 2003/0106484) teaches a method for manufacturing a silicon wafer, in which a silicon wafer has been sliced from a silicon single crystal, and the silicon wafer is heat treated in an oxidizing atmosphere (See paragraphs [0013] and [0030])

Furthermore, Fusegawa ('454) disclose a silicon wafer manufactured from a silicon single crystal having high interstitial oxygen concentration is subjected to a heat treatment process, for example, at high temperature of 1150°C in an oxidizing atmosphere for about 2 hrs [See paragraph 13]. Furthermore, Fusegawa et al ('454) disclose the concentration of interstitial oxygen in a silicon single crystal wafer is 6×10^{17} to 10×10^{17} atoms $/cm^3$ [See paragraph (0030)] wherein the concentration of interstitial oxygen was measured by FT-IR (Fourier Transform Infrared Spectroscopy) [See paragraph 85]. Fusegawa et al ('484) also teach the silicon single crystal can be processed into a wafer of the present invention by subjecting it to slicing and mirror-finish-polishing [See paragraph (0074)]. Moreover, Fusegawa et al ('484) also teaches the silicon ingot can be processed into a wafer by subjecting it to slicing and mirror-finish-polishing [See paragraph (0074)].

However, Fusegawa et al ('454) does not teach the relationship between interstitial oxygen concentration and heat treatment temperature.

In the analogous art, JP (2003-297840) teaches a method of manufacturing silicon wafer by applying a heat treatment process in an oxygen content atmosphere wherein the interstitial oxygen concentration [Oi] of silicon wafer has following relationship with the temperature:

$$[O_i] < [O_i]^{eq}(T)\exp(\frac{2\sigma_{SiO2}\Omega}{rkT})$$

Where $[O_i]$ is the concentration of the interstitial oxygen $[O_i]^{eq}$ is the concentration of interstitial oxygen at equilibrium temperature, (T) is equilibrium

temperature, σ_{SiO2} is the surface energy of silicon oxide, σ is the volume of the depositing oxygen atom, r expresses an average COP, k is a Boltzman constant, and T is heat treatment temperature. (See paragraph [0021] and [0022])

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to increase confidence level in overall process control for manufacturing method of silicon wafer of Fusegawa et al. ('484) by providing a relationship between interstitial oxygen concentration [Oi] and temperature [T] in order to measure the strength of silicon wafer since oxygen concentration is effective for enhancing the strength of a silicon wafer, as suggested by JP (2003-297840).

Claims 21 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fusegawa et al ('484) and JP (2003-297840) and further in view of Haas et al (US 4,119,441)

Hypothetical combined teachings of Fusegawa et al ('484) and Wakabayashi et al ('737) disclose all the limitations of a manufacturing method of a silicon single crystal wafer but do not teach that single crystal used to manufacture of silicon wafer is doped with phosphorus through a neutron irradiation.

In the analogous art, Haas et al ('441) disclose a method for the production of n-doped silicon single crystals wherein the silicon single crystal is exposed to a pattern of radiation. The neutron radiation causes a doping concentration in marginal regions of the crystal due to the production of phosphorus atoms [See abstract].

It would have been obvious to one of ordinary skill in this art at the time of applicant's invention to dope silicon wafer manufactured by hypothetical combined

teachings method of Fusegawa et al ('484) and JP (2003-297840) with phosphorus by using a neutron irradiation in order to decrease crystal damage and making a specific resistance in the silicon single crystal as suggested by Haas et al ('441).

Claims 22 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fusegawa et al ('484) and JP (2003-297840) and further in view of Asayama et al (US 6,641,888).

Hypothetical combined teachings of Fusegawa et al ('484) and JP (2003-297840) disclose all the limitations of a manufacturing method of a silicon single crystal wafer as discussed above but do not teach that single crystal used to manufacture of silicon wafer is doped with nitrogen by a concentration of 2×10^{13} $atoms/cm^3$ or more and/or with carbon by a concentration of 5×10^{16} $atoms/cm^3$ or more.

In the analogous art, Asayama et al. ('888) present an invention which relates to a silicon single crystal used for a semiconductor integrated circuit device and to a silicon wafer and an epitaxial wafer [See lines 9-15, column 1]. Further, Asayama et al. ('888) discloses the silicon single crystal is grown with nitrogen doping at a concentration of 1×10^{13} $atoms/cm^3$ or more, or with nitrogen doping at a concentration of 1×10^{12} $atoms/cm^3$ and carbon doping at a concentration of 0.1×10^{16} - 5×10^{16} $atoms/cm^3$ [See abstract].

Therefore, It would have been obvious to one of ordinary skill in this art at the time of applicant's invention to dope silicon wafer manufactured by hypothetical combined teachings method of Fusegawa et al ('484) and JP (2003-297840) with

nitrogen and carbon in order to control the resistance of the silicon single crystal as suggested by Asayama et al. ('441).

Claims 28, 32, 36, 40, and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fusegawa et al ('484), and JP (2003-297840) and further in view of prior art submitted by the applicants Momoi et al (US 2002/0024152).

Hypothetical combined teachings of Fusegawa et al ('484) and JP (2003-297840) disclose all the claim limitations of manufacturing method of a silicon single crystal wafer as discussed above but do not teach the manufacturing method of SOI wafer.

In the analogous art, Momoi et al. (US 2002/0024152) discloses a method of manufacturing an SOI wafer wherein the SOI wafer includes a substrate, a buried insulating layer formed on substrate, and single-crystal semiconductor layer formed on buried insulating layer. (See paragraphs [0113], [0118], and [0190])

Further, Momoi et al. ('152) teaches buried oxide film is formed On the SOI wafer by applying a heat treatment to an active layer side silicon wafer (See paragraphs [0138] and [0139]).

Further, Momoi et al. ('152) teaches silicon wafer is then bonded to a supporting side wafer with said buried oxide layer interposed therebetween to manufacture a bonded SOI wafer. (See paragraphs [0151] and [0189])

Moreover, Momoi et al. ('152) teaches forming an ion implanted layer in active layer side silicon wafer by forming an oxide film on active layer side silicon wafer, and ion-implanting via said oxide film. (See paragraphs [0168] and [0171])

Further, Momoi et al. ('152) teach seperating a part of active layer side silicon wafer from a boundary defined by ion implanted layer. (See paragraph [0151] and [0154])

It would have been obvious to one of ordinary skill in this art at the time of applicant's invention to modify silicon wafer manufactured by hypothetical combined teachings method of Fusegawa et al ('484) and JP (2003-297840) through manufacturing a SOI wafer in order to reduce signal transmission loss of a semiconductor device by providing SOI substrate in the semiconductor system, as suggested by Momoi et al. (US 2002/0024152).

Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fusegawa et al ('484), JP (2003-297840), Haas et al (US 4,119,441) and further in view of prior art submitted by the applicants, Momoi et al. (US 2002/0024152)

Hypothetical combined teachings of Fusegawa et al ('484), JP (2003-297840), and Haas et al (US 4,119,441) disclose all the claim limitations of a manufacturing method of a silicon single crystal wafer as discussed above but do not teach the manufacturing method of SOI wafer.

In the analogous art, Momoi et al. (US 2002/0024152) discloses a method of manufacturing an SOI wafer wherein the SOI wafer includes a substrate, a buried insulating layer formed on substrate, and single-crystal semiconductor layer formed on buried insulating layer. (See paragraphs [0113], [0118], and [0190])

It would have been obvious to one of ordinary skill in this art at the time of applicant's invention to modify silicon wafer manufactured by hypothetical combined

teachings method of Fusegawa et al ('484), JP (2003-297840), Haas et al (US 4,119,441) through manufacturing a SOI in order to reduce signal transmission loss of a semiconductor device by providing SOI substrate in the system, as suggested by Momoi et al ('152).

Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fusegawa et al ('484), JP (2003-297840), Asayama et al (US 6,641,888) and further in view of prior art submitted by the applicants, Momoi et al. (US 2002/0024152)

Hypothetical combined teachings of Fusegawa et al ('484), JP (2003-297840), and Haas et al (US 4,119,441) disclose all the claim limitations of manufacturing method of a silicon single crystal wafer as discussed above but do not teach the manufacturing method of SOI wafer.

In the analogous art, Momoi et al. (US 2002/0024152) discloses a method of manufacturing an SOI wafer wherein the SOI wafer includes a substrate, a buried insulating layer formed on substrate, and single-crystal semiconductor layer formed on buried insulating layer. (See paragraphs [0113], [0118], and [0190])

It would have been obvious to one of ordinary skill in this art at the time of applicant's invention to modify silicon wafer manufactured by hypothetical combined teaching method of Fusegawa et al ('484), JP (2003-297840), Asayama et al (US 6,641,888) through manufacturing a SOI wafer in order to reduce signal transmission loss of a semiconductor device by providing SOI substrate in the system, as suggested by Momoi et al. (US 2002/0024152)

Claims 33, 37, and 42-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fusegawa et al ('484), JP (2003-297840), Momoi et al. ('152) and further in view of Haas et al (US 4,119,441).

Hypothetical combined teachings of Fusegawa et al ('484), JP (2003-297840), and Momoi et al. ('152) disclose all the limitations of a manufacturing method of a SOI wafer from a silicon single crystal wafer as discussed above but do not teach that single crystal used to manufacture of SOI wafer is doped by phosphorus through a neutron irradiation.

In the analogous art, Haas et al ('441) disclose a method for the production of n-doped silicon single crystals wherein the silicon single crystal is exposed to a pattern of radiation. The neutron radiation causes a weaker doping concentration in marginal regions of the crystal due to the production of fewer phosphorus atoms [See abstract].

It would have been obvious to one of ordinary skill in this art at the time of applicant's invention to dope active layer side of silicon wafer used to manufacture SOI wafer by hypothetical combined teaching method of Fusegawa et al ('484), JP (2003-297840), and Momoi et al. ('152) with phosphorus by using a neutron irradiation in order to decrease crystal damage and making a specific resistance in the silicon single crystal, as suggested by Haas et al ('441).

Claims 34, 38, 44-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fusegawa et al ('484), JP (2003-297840), Momoi et al. ('152), and further in view of Asayama et al (US 6,641,888).

Hypothetical combined teaching of Fusegawa et al ('484), JP (2003-297840), and Momoi et al. ('152) disclose all the claim limitations of a manufacturing method of a SOI wafer from a silicon single crystal wafer as discussed above but do not teach that single crystal of SOI wafer is doped with nitrogen by a concentration of 2×10^{13} $atoms/cm^3$ or more and/or with carbon by a concentration of 5×10^{16} $atoms/cm^3$ or more.

In the analogous art, Asayama et al. ('888) present an invention which relates to a silicon single crystal used for a semiconductor integrated circuit device and to a silicon wafer and an epitaxial wafer [See lines 9-15, column 1]. Further, Asayama et al. ('888) disclose the silicon single crystal is suitable for an epitaxial wafer is grown with nitrogen doping at a concentration of 1×10^{13} $atoms/cm^3$ or more, or with nitrogen doping at a concentration of 1×10^{12} $atoms/cm^3$ and carbon doping at a concentration of 0.1×10^{16} - 5×10^{16} $atoms/cm^3$ [See abstract].

It would have been obvious to one of ordinary skill in this art at the time of applicant's invention to dope active layer side of silicon wafer used to manufacture SOI wafer by hypothetical combined teaching method of Fusegawa et al ('484), JP (2003-297840), and Momoi et al. ('152) with nitrogen and carbon in order to control the resistance of the silicon single crystal as suggested by Asayama et al. ('441)

Response to Arguments

Applicant's arguments with respect to claim 20-22, 24-26, 28-30, 32-34, 36-38, and 40-45 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Seyed Masoud Malekzadeh whose telephone number is 571-272-6215. The examiner can normally be reached on Monday – Friday at 8:30 am – 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Yogendra N. Gupta can be reached on (571) 272-1316. The fax number for the organization where this application or proceeding is assigned is 571-272-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published application may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance form a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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